Amendments to the Claims

1. (Cancelled)

2. (Previously Presented) The device as in Claim 56, wherein the packaged semiconductor is packaged in a ball grid array package.

3. (Previously Presented) The device as in Claim 56, wherein the unpackaged semiconductor die is a graphics processor.

4. (Previously Presented) The device as in Claim 56, wherein the packaged semiconductor is a memory.

5. (Previously Presented) The device as in Claim 56, wherein a plurality of packaged semiconductors are attached to the package module.

6. (Previously Presented) The device as in Claim 56, wherein the unpackaged semiconductor die is wire bonded to the package module.

7. (Currently amended) The device as in Claim [1] 57, wherein the unpackaged semiconductor die is wire bonded to the package module.

8. (Previously Presented) The device as in Claim 56, wherein attached includes surface-mount technology reflow.

9. (Previously Presented) The device as in Claim 56, wherein the encapsulated structure has a footprint greater than the footprint of the unpackaged semiconductor die.

10. (Currently amended) The device in Claim [1] 56, wherein the unpackaged semiconductor die is underfilled.

11. (Previously Presented) The device as in Claim 56, wherein the footprint size of the package module is one of 35 mm × 35 mm, 31 mm × 31 mm, 27 mm × 27 mm, 37.5 mm × 37.5 mm, 40 mm × 40 mm, 42 mm × 42 mm, or 42.5 mm × 42.5 mm.

12. (Previously Presented) The device as in Claim 56, further including a heat sink.

13. (Previously Presented) The device in Claim 12, wherein a top surface of the unpackaged semiconductor die and a top surface of the packaged semiconductor are of substantially equal distance from a surface of the package module.

14. (Currently amended) The device as in Claim [12] 59, further including a shim positioned over the unpackaged semiconductor die such that a top of the shim and a top surface of the packaged semiconductor are of substantially equal distance from a surface of the multi-die module.

15. (Cancelled).

16. (Previously Presented) The device as in Claim 56, wherein the packaged semiconductor die is packaged in a ball grid array package.

17. (Previously Presented) The device as in Claim 57, wherein a plurality of packaged memory are attached to the package module.

18. (Previously Presented) The device as in Claim 57, wherein directly attached includes the graphics processing die being wire bonded to the package module.

19. (Currently amended) The device as in Claim [15] 59, wherein directly attached includes flip-chip attachment.

20. (Previously Presented) The device as in Claim 57, wherein attached includes surface-mount technology reflow.

21. (Cancelled)

22. (Currently amended) The device as in Claim [15] 57, wherein the graphics-processing die is underfilled.

23. (Previously Presented) The device as in Claim 57, wherein the standard package sizes include one of 35 mm × 35 mm, 31 mm × 31 mm, 27 mm × 27 mm, 37.5 mm × 37.5 mm, 40 mm × 40 mm, 42 mm × 42 mm, or 42.5 mm × 42.5 mm.

24. (Previously presented) The device as in Claim 57, further including a heat sink.

25. (Previously Presented) The device in claim 24, wherein a top surface of the graphics-processor die and a top surface of the packaged memory are of substantially equal distance from a surface of the package module.

26. (Currently Amended) The device as in Claim [24] 57, further including a shim positioned on top of the graphics-processor die such that a top of the shim and a top surface of the packaged memory are of substantially equal distance from a surface of the package module.

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Cancelled)

35. (Cancelled)

36. (Cancelled)

37. (Cancelled)

38. (Cancelled)

39. (Cancelled)

40. (Cancelled)

41. (Previously Presented) The device as in Claim 9, wherein the encapsulated semiconductor die forms a substantially rectangular structure on the package module.

42. (Previously Presented) The device of Claim 22, wherein the encapsulated graphics-processing die forms a substantially rectangle structure on the package module

43. (Cancelled)

44. (Previously Presented) The multi-die module as in Claim 58, further including a second packaged semiconductor die mounted on the first surface of the substrate.

45. (Previously Presented) The multi-die module as in Claim 58, further including a plurality of unpackaged semiconductor die mounted on the first surface of the substrate.

46. (Previously Presented) The multi-die module as in Claim 58, wherein the unpackaged semiconductor die is mounted to the first surface of the substrate by wire bonding.

47. (Previously Presented) The multi-die module as in Claim 58, wherein the encapsulating structure is further comprised of an encapsulating material including epoxy, metal cap or silicon coatings.

48. (Previously Presented) The multi-die module as in Claim 58, further including a heat sink.

49. (Cancelled)

50. (Previously Presented) The multi-die module as in Claim [43] 59, wherein the unpackaged semiconductor die is under filled.

51. (Cancelled)

52. (Previously Presented) The multi-die as in Claim [51] 56, further including a shim positioned over the surface of the unpackaged semiconductor die such as that atop of the shim and the top surface of the packaged semiconductor die are of substantially equal distance from the first surface of the substrate.

53. (Previously Presented) The multi-die module as in Claim 58, wherein the unpackaged semiconductor die is a graphics processor.

54. (Previously Presented) The multi-die module as in Claim 58, wherein the packaged semiconductor die is a memory.

55. (Cancelled)

56. (Previously Presented) A device comprising:

a package module including a substrate having a standard package footprint;

an unpackaged semiconductor die directly attached to the package module, the unpackaged semiconductor die encapsulated onto the package module in a structure having a planar top surface; and

a packaged semiconductor die having a top surface and attached to the package module;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

57. (Previously Presented) A device comprising:

a package module sized to be interchangeable with standard package sizes;

a graphics-processing die directly attached to the package module, the graphics-processing die encapsulated on the package module in a structure having a planar top surface; and

a packaged memory die having a top surface and attached to the package module; wherein the planar top surface of the encapsulated structure and the top surface of the packaged memory die are of equal distance from the package module.

58. (Previously Presented) A multi-die module, comprising:

a substrate having a first surface and a second surface;

an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a planar top surface; and

a packaged semiconductor die having a top surface and mounted on the first surface of the substrate;

wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

59. (Currently Amended) A multi-die module, comprising:

a substrate having a first surface;

an unpackaged semiconductor die mounted to the first surface of the substrate, the semiconductor die encapsulated in a structure having a planar top surface; and

a packaged semiconductor die having a top surface and mounted on the first surface of the substrate ~~wherein the encapsulating structure is further comprised of an encapsulating material of a metal cap~~ wherein the planar top surface of the encapsulated structure and the top surface of the packaged semiconductor die are of equal distance from the substrate.

60. (Currently Amended) The device of claim 56 further including a planar heat sink adapted to engage the encapsulated structure and the top surface of the packaged semiconductor.